Electronic Version
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Claims

[c1] 1.An offsetting phase-locked loop (PLL) comprising:
a primary phase comparator, receiving a reference clock and a primary feedback clock;
a primary filter capacitor for generating a primary filter voltage;
a primary charge pump, activated by phase differences detected by the primary phase comparator, for charging and discharging the primary filter capacitor;
a primary voltage-controlled oscillator (VCO) for generating a primary output clock having an output frequency that is a function of a primary VCO input voltage of a primary VCO input;
an op amp having a first input receiving the primary filter voltage, and an output driving the primary VCO input;
an offset resistor, coupled between the primary VCO input and a second input to the op amp;
a digital-to-analog converter (DAC) receiving a digital value, for generating a DAC current as a function of the digital value, the DAC current being driven through the offset resistor;
a secondary phase comparator, receiving the reference clock and a secondary feedback clock;

a secondary filter capacitor for generating a secondary filter voltage;

a secondary charge pump, activated by phase differences detected by the secondary phase comparator, for charging and discharging the secondary filter capacitor;

a secondary voltage-controlled oscillator (VCO) for generating a secondary output clock having an output frequency that is a function of the secondary filter voltage; and

a coupling switch, between the secondary VCO and the primary phase comparator, for coupling the secondary output clock to the primary feedback clock after the DAC generates the DAC current,

whereby the DAC generates the DAC current to offset a voltage of the primary VCO input.

[c2] 2.The offsetting phase-locked loop of claim 1 wherein the primary output clock or a derivative of the primary output clock is fed back to the primary phase comparator as the primary feedback clock;

wherein the secondary output clock or a derivative of the secondary output clock is fed back to the secondary phase comparator as the secondary feedback clock.

[c3] 3.The offsetting phase-locked loop of claim 2 further comprising:

a primary switch, coupled between the primary output

clock and the primary feedback clock, for disconnecting the primary output clock from the primary feedback clock.

[c4] 4.The offsetting phase-locked loop of claim 3 wherein the primary switch opens, disconnecting the primary VCO from the primary phase comparator, when the DAC initially generates the DAC current.

[c5] 5.The offsetting phase-locked loop of claim 4 wherein the coupling switch opens, disconnecting the secondary VCO from the primary phase comparator, when the DAC initially generates the DAC current.

[c6] 6.The offsetting phase-locked loop of claim 2 wherein the first input to the op amp is a non-inverting input and the second input to the op amp is an inverting input.

[c7] 7.The offsetting phase-locked loop of claim 2 wherein the primary output clock is the primary feedback clock or is a multiple of the primary feedback clock.

[c8] 8.The offsetting phase-locked loop of claim 2 further comprising:
a primary feedback divider between the primary output clock and the primary feedback clock;
wherein the primary output clock is a multiple of the primary feedback clock.

[c9] 9.A dual-loop phase-locked loop (PLL) comprising:

a first loop that comprises:

a first phase comparator that receives a reference clock and a first feedback clock;

a first filter capacitor on a first filter node;

a first charge pump, coupled to the first phase comparator and to the first filter node, for charging and discharging the first filter capacitor;

a first oscillator for generating a first output clock in response to a first control node;

wherein the first output clock or a derivative is fed back to the first phase comparator as the first feedback clock;

a digital-to-analog converter (DAC) receiving a digital value and outputting an analog voltage generated in response to the digital value;

an op amp, coupled between the first filter node and the first control node;

a resistor coupled to receive the analog voltage from the DAC, the resistor coupled between a second input of the op amp and the first control node;

a second loop that comprises:

a second phase comparator that receives the reference clock and a second feedback clock;

a second filter capacitor on a second filter node;

a second charge pump, coupled to the second phase

comparator and to the second filter node, for charging and discharging the second filter capacitor;
a second oscillator for generating a second output clock in response to the second filter node;
wherein the second output clock or a derivative is fed back to the second phase comparator as the second feedback clock; and
a coupling switch coupled between the second oscillator and the first phase comparator.

[c10] 10.The dual-loop phase-locked loop of claim 9 further comprising:
an isolating switch for disconnecting the first oscillator from the first phase comparator.

[c11] 11.The dual-loop phase-locked loop of claim 10 wherein the coupling switch is closed to connect the second loop to the first loop when the digital value to the DAC changes.

[c12] 12.The dual-loop phase-locked loop of claim 11 wherein the second input to the op amp is an inverting input, the op amp having a non-inverting input coupled to the first filter node and an output driving the first control node.

[c13] 13.The dual-loop phase-locked loop of claim 12 wherein a frequency of the first output clock is a function of a

voltage of the first control node;
wherein a frequency of the second output clock is a function of a voltage of the second filter node,
wherein the first and second oscillator are voltage-controlled oscillators (VCOs).

[c14] 14.A reference-tracking and frequency-offsetting clock generator comprising:
first phase comparator means, receiving a reference clock and a first feedback clock, for comparing phases of the reference clock and the first feedback clock;
first filter capacitor means, on a first filter node, for storing charge;
first charge pump means, coupled to the first phase comparator means and to the first filter node, for charging and discharging the first filter capacitor means;
first oscillator means for generating a first output clock in response to a first control node;
first feedback means, receiving the first output clock, for feeding back the first output clock or a derivative to the first phase comparator means as the first feedback clock;
digital-to-analog converter DAC means, receiving a digital value, for converting the digital value to an analog current;
op amp means, coupled between the first filter node and the first control node, for driving the first control node in

response to a difference between a first input and a second input, the first input coupled to the first filter node;
resistor means, coupled between the second input of the op amp means and the first control node, for generating an offset voltage across the op amp means in response to the analog current from the DAC means;
wherein the offset voltage is a voltage difference between the first filter node and the first control node that results in a frequency offset of the first output clock;
second phase comparator means, receiving the reference clock and a second feedback clock, for comparing phases of the reference clock and the second feedback clock;
second filter capacitor means, on a second filter node, for storing charge;
second charge pump means, coupled to the second phase comparator means and to the second filter node, for charging and discharging the second filter capacitor means;
second oscillator means for generating a second output clock in response to the second filter node;
second feedback means, receiving the second output clock, for feeding back the second output clock or a derivative to the second phase comparator means as the second feedback clock; and
coupling means, between the first feedback clock and

the second output clock, for connecting the second output clock to the first feedback clock to the first phase comparator means when the DAC means adjusts the analog current in response to changes in the digital value.

[c15] 15.The reference-tracking and frequency-offsetting clock generator of claim 14 further comprising:
isolating switch means for disconnecting the first oscillator means from the first phase comparator means when the digital value is applied to the DAC means.

[c16] 16.The reference-tracking and frequency-offsetting clock generator of claim 14 wherein the coupling means further comprises:
switch means for applying the second output clock as the first feedback clock to the first phase comparator means after the DAC means has adjusted the analog current;
wherein second output clock adjusts a frequency of the first output clock to account for changes to the reference clock during a time when the DAC means adjusted the analog current.

[c17] 17.The reference-tracking and frequency-offsetting clock generator of claim 14 wherein the second input to the op amp means is an inverting input, and the first in-

put to the op amp means is a non-inverting input.